查询LT1150供应商



# ±15V Chopper Stabilized Operational Amplifier with Internal Capacitors

## FEATURES

- High Voltage Operation, ±18V
- No External Components Required
- Maximum Offset Voltage 5μV
- Maximum Offset Voltage Drift 0.05μV/°C
- Low Noise 1.8μVp-p (0.1Hz to 10Hz)
- Minimum Voltage Gain 140dB
- Minimum PSRR 120dB
- Minimum CMRR 120dB
- Low Supply Current 0.8mA
- Single Supply Operation 4.75V to 36V
- Input Common Mode Range Includes Ground
- 200μA Supply Current with Pin 1 Grounded
- Typical Overload Recovery Time 20ms

## APPLICATIONS

- Strain Gauge Amplifiers
- Electronic Scales
- Medical Instrumentation
- Thermocouple Amplifiers
- High Resolution Data Acquisition

## DESCRIPTION

The LTC1150 is a high-voltage, high-performance chopper stabilized operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper amplifiers are integrated on-chip. Further, LTC's proprietary high-voltage CMOS structures allow the LTC1150 to operate at up to 36V total supply voltage.

The LTC1150 has an offset voltage of 0.5μV, drift of 0.01μV/°C, 0.1Hz to 10Hz input noise voltage of 1.8μVp-p and a typical voltage gain of 180dB. The slew rate of 3V/μs and a gain bandwidth product of 2.5MHz are achieved with 0.8mA of supply current. Overload recovery times from positive and negative saturation conditions are 3ms and 20ms, respectively.

For applications demanding low power consumption, pin 1 can be used to program the supply current. Pin 5 is an optional AC-coupled clock input, useful for synchronization.

The LTC1150 is available in a standard 8-lead metal can, plastic and ceramic dual in line packages, as well as an 8-lead SO8 package. The LTC1150 can be a plug-in replacement for most standard bipolar op amps with significant improvement in DC performance.

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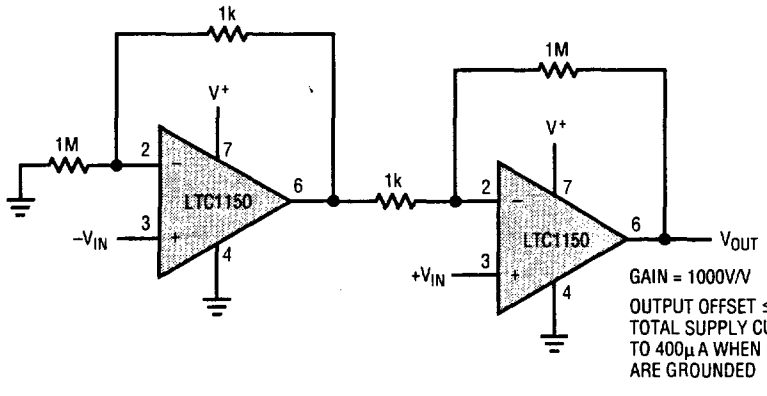
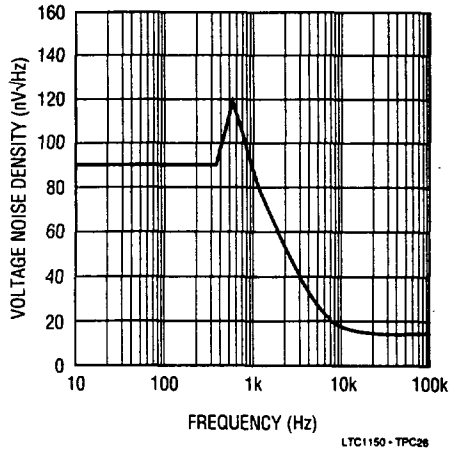
## TYPICAL APPLICATION

**Single Supply Instrumentation Amplifier**




**Noise Spectrum**

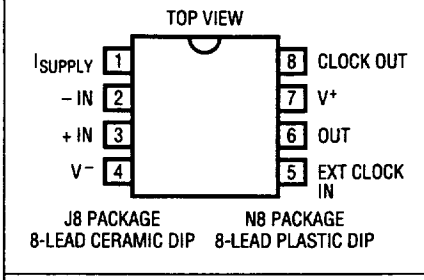


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

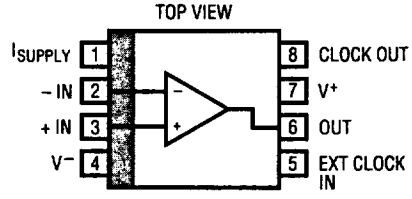
Total Supply Voltage ($V^+$ to $V^-$) ..... 36V
Input Voltage (Note 2) ..... ($V^+$ + 0.3V) to ($V^-$ – 0.3V)
Output Short Circuit Duration ..... Indefinite
Burn-In Voltage ..... 36V
Operating Temperature Range
LTC1150M ..... –55°C to 125°C
LTC1150C ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

## PACKAGE/ORDER INFORMATION




J8 PACKAGE
8-LEAD CERAMIC DIP

N8 PACKAGE
8-LEAD PLASTIC DIP




S8 PACKAGE
8-LEAD PLASTIC SOIC

| ORDER PART NUMBER |
|---|
| LTC1150MJ8<br>LTC1150CJ8<br>LTC1150CN8 |
| LTC1150CS8 |
| S8 PART MARKING |
| 1150 |

## ELECTRICAL CHARACTERISTICS

**$V_S$ = ±15V, Pin 1 = Open, $T_A$ = Operating Temperature Range, unless otherwise specified.**

| PARAMETER | CONDITIONS | | LTC1150M MIN | LTC1150M TYP | LTC1150M MAX | LTC1150C MIN | LTC1150C TYP | LTC1150C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $T_A$ = 25°C (Note 3) | | | ±0.5 | ±5 | | ±0.5 | ±5 | µV |
| Average Input Offset Drift | (Note 3) | ● | | ±0.01 | ±0.05 | | ±0.01 | ±0.05 | µV/°C |
| Long Term Offset Voltage Drift | | | | 50 | | | 50 | | nV/√mo |
| Input Offset Current | $T_A$ = 25°C | | | ±20 | ±60 | | ±20 | ±200 | pA |
| | | ● | | | ±1.5 | | | ±0.5 | nA |
| Input Bias Current | $T_A$ = 25°C | | | ±10 | ±50 | | ±10 | ±100 | pA |
| | | ● | | | ±2.5 | | | ±0.5 | nA |
| Input Noise Voltage | $R_S$ = 100Ω, 0.1Hz to 10Hz, TC2 | | | 1.8 | | | 1.8 | | µVp-p |
| | $R_S$ = 100Ω, 0.1Hz to 1Hz, TC2 | | | 0.6 | | | 0.6 | | |
| Input Noise Current | f = 10Hz (Note 4) | | | 1.8 | | | 1.8 | | fA/√Hz |
| Common-Mode Rejection Ratio | $V_{CM}$ = $V^-$ to 12V | ● | 110 | 130 | | 110 | 130 | | dB |
| Power Supply Rejection Ratio | $V_S$ = ±2.375V to ±16V | ● | 120 | 145 | | 120 | 145 | | dB |
| Large Signal Voltage Gain | $R_L$ = 10kΩ, $V_{OUT}$ = ±10V | ● | 140 | 180 | | 140 | 180 | | dB |
| Maximum Output Voltage Swing | $R_L$ = 10kΩ $T_A$ = 25°C | | ±13.5 | ±14.5 | | ±13.5 | ±14.5 | | V |
| | $R_L$ = 10kΩ | ● | +10.5/ –13.5 | | | +10.5/ –13.5 | | | |
| | $R_L$ = 100kΩ | | | ±14.95 | | | ±14.95 | | |
| Slew Rate | $R_L$ = 10kΩ, $C_L$ = 50pF | | | 3 | | | 3 | | V/µs |
| Gain Bandwidth Product | | | | 2.5 | | | 2.5 | | MHz |
| Supply Current | No Load $T_A$ = 25°C | | | 0.8 | 1.0 | | 0.8 | 1.5 | mA |
| | No Load, Pin 1 = $V^-$ $T_A$ = 25°C | | | 0.2 | | | 0.2 | | |
| | No Load | ● | | | 1.5 | | | 2 | |
| Internal Sampling Frequency | | | | 550 | | | 550 | | Hz |

# ELECTRICAL CHARACTERISTICS

**$V_S$ = 5V, Pin 1 = Open, $T_A$ = Operating Temperature Range, unless otherwise specified.**

| PARAMETER | CONDITIONS | | LTC1150M MIN | LTC1150M TYP | LTC1150M MAX | LTC1150C MIN | LTC1150C TYP | LTC1150C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Input Offset Voltage | $T_A$ = 25°C (Note 3) | | | ±0.5 | ±5 | | ±0.05 | ±5 | µV |
| Average Input Offset Drift | (Note 3) | ● | | ±0.01 | ±0.05 | | ±0.01 | ±0.05 | µV/°C |
| Long Term Offset Voltage Drift | | | | 50 | | | 50 | | nV/√mo |
| Input Offset Current | $T_A$ = 25°C | | | ±10 | ±30 | | ±10 | ±60 | pA |
| | | ● | | | ±100 | | | ±100 | |
| Input Bias Current | $T_A$ = 25°C | | | ±5 | ±15 | | ±5 | ±30 | pA |
| | | ● | | | ±400 | | | ±100 | |
| Input Noise Voltage | $R_S$ = 100Ω, 0.1Hz to 10Hz, TC2 | | | 2.0 | | | 2.0 | | µVp-p |
| | $R_S$ = 100Ω, 0.1Hz to 1Hz, TC2 | | | 0.7 | | | 0.7 | | |
| Input Noise Current | f = 10Hz (Note 4) | | | 1.3 | | | 1.3 | | fA/√Hz |
| Common-Mode Rejection Ratio | $V_{CM}$ = 0V to 2.7V | ● | 110 | | | 110 | | | dB |
| Power Supply Rejection Ratio | $V_S$ = ±2.375V to ±16V | ● | 130 | 145 | | 125 | 145 | | dB |
| Large Signal Voltage Gain | $R_L$ = 10kΩ, $V_{OUT}$ = 0.3V to 4.5V | ● | 130 | 180 | | 130 | 180 | | dB |
| Maximum Output Voltage Swing | $R_L$ = 10kΩ | | | 0.15 – 4.85 | | | 0.15 – 4.85 | | V |
| | $R_L$ = 100kΩ | | | 0.02 – 4.97 | | | 0.02 – 4.97 | | |
| Slew Rate | $R_L$ = 10kΩ, $C_L$ = 50pF | | | 1.5 | | | 1.5 | | V/µs |
| Gain Bandwidth Product | | | | 1.8 | | | 1.8 | | MHz |
| Supply Current | No Load $T_A$ = 25°C | | | 0.4 | 1 | | 0.4 | 1 | mA |
| | | ● | | | 1.5 | | | 1.5 | |
| Internal Sampling Frequency | | | | 300 | | | 300 | | Hz |

The ● denotes the specifications which apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which life of the device may be impaired.

**Note 2:** Connecting any terminal to voltages greater than $V^+$ or less than $V^-$ may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1150.

**Note 3:** These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high-speed automatic test systems. $V_{OS}$ is measured to a limit determined by test equipment capability.

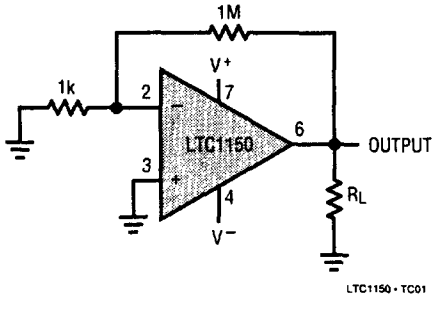
**Note 4:** Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \bullet I_b)}$$

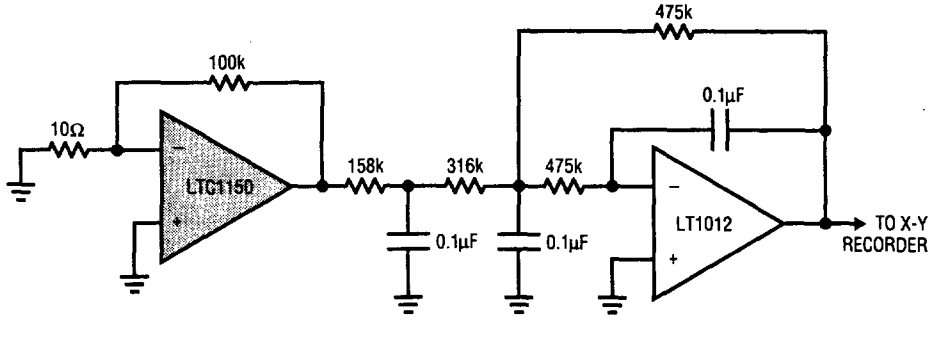
where $q = 1.6 \times 10^{-19}$ Coulomb.

# TEST CIRCUITS

**Offset Voltage Test Circuit**




**DC-10Hz Noise Test Circuit**

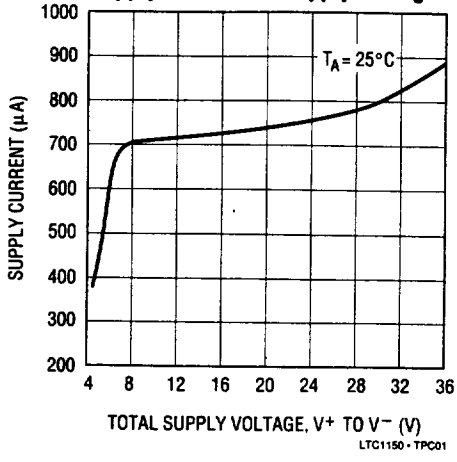



FOR 1Hz NOISE BW, INCREASE ALL THE CAPACITORS BY A FACTOR OF 10.

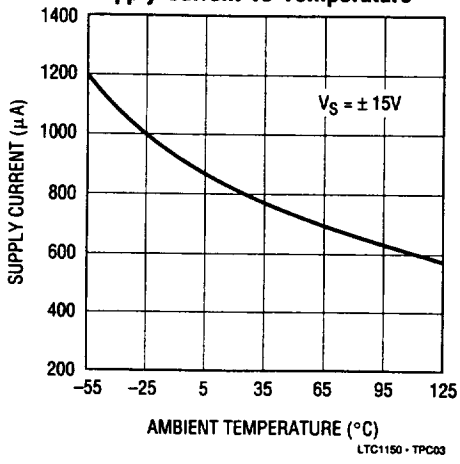
LTC1150 • TC02

# TYPICAL PERFORMANCE CHARACTERISTICS

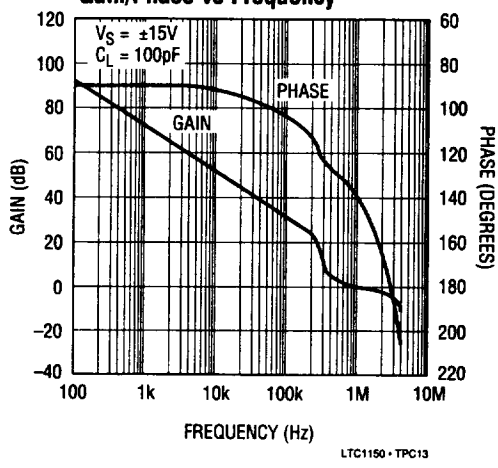
**Supply Current vs Supply Voltage**



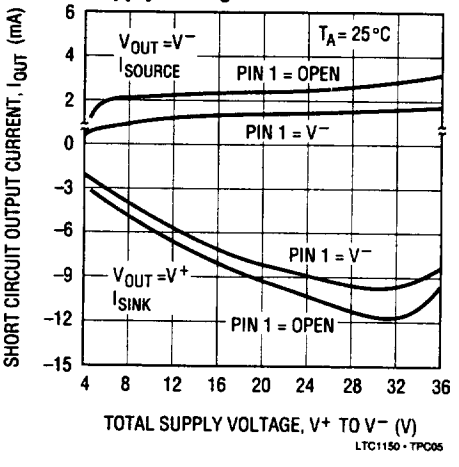

**Supply Current vs Temperature**



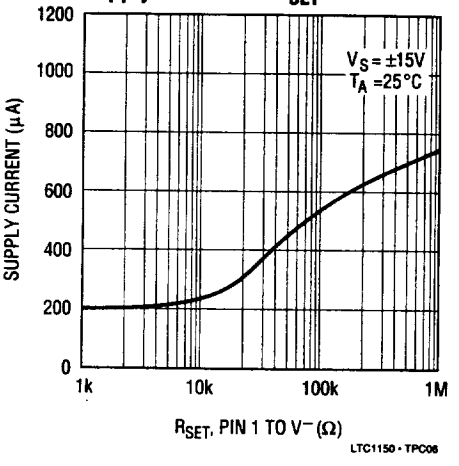

**Gain/Phase vs Frequency**



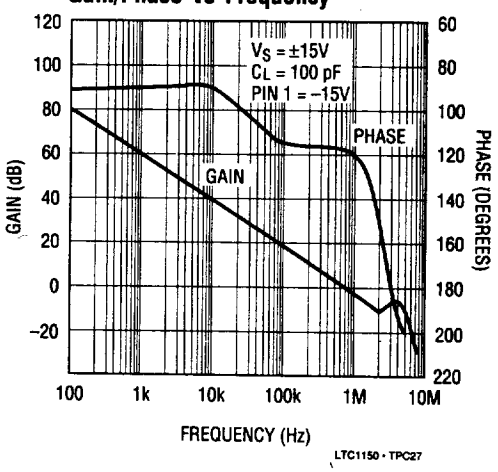

**Output Short Circuit Current vs Supply Voltage**



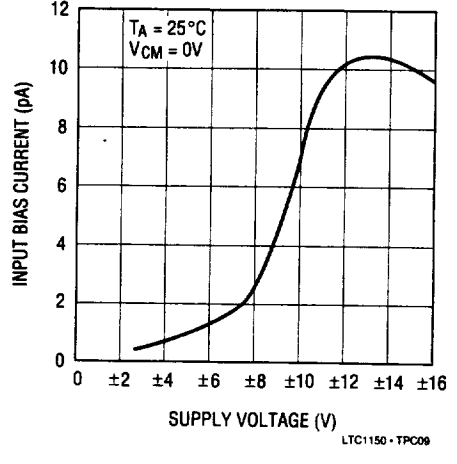

**Supply Current vs $R_{SET}$**



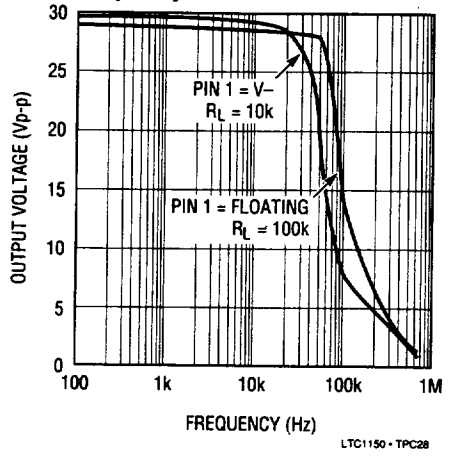

**Gain/Phase vs Frequency**



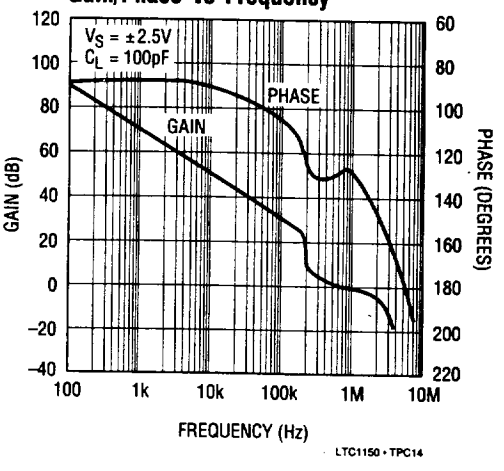

**Input Bias Current vs Supply Voltage**




**Undistorted Output Swing vs Frequency**




**Gain/Phase vs Frequency**

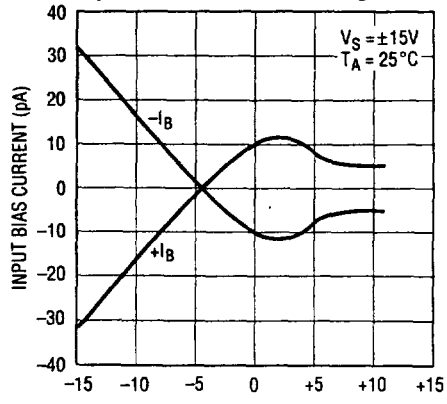




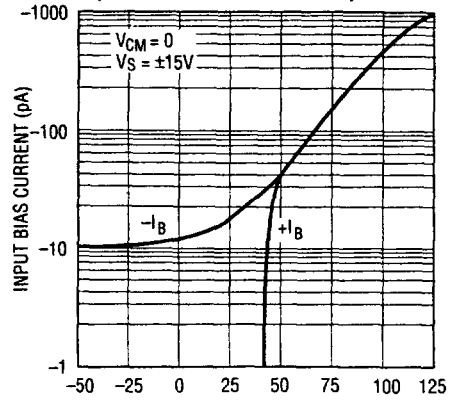

LINEAR TECHNOLOGY

# TYPICAL PERFORMANCE CHARACTERISTICS

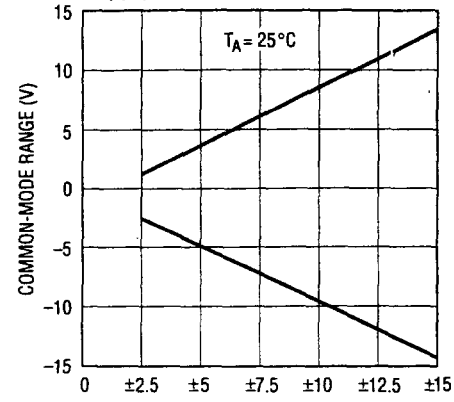
**Input Bias Current vs Input Common-Mode Voltage**




**Input Bias Current vs Temperature**

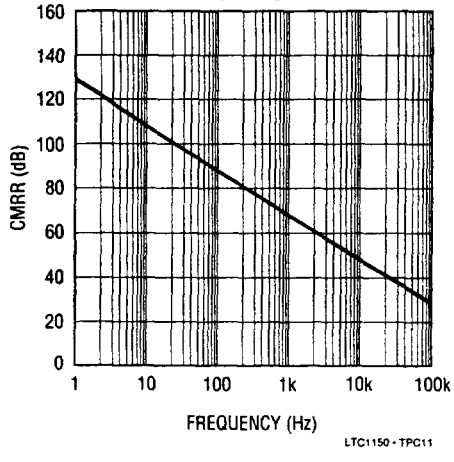



**Common-Mode Input Range vs Supply Voltage**

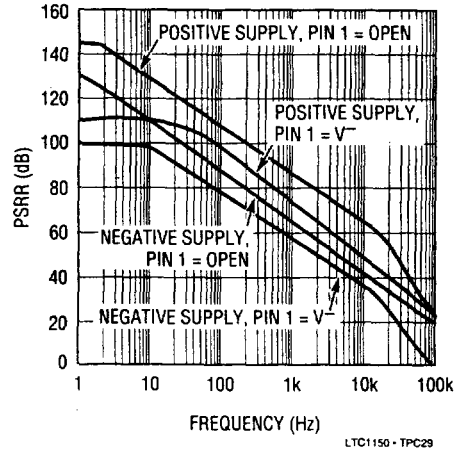



2

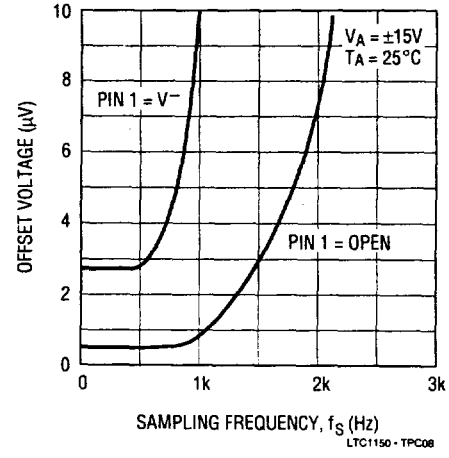
**CMRR vs Frequency**



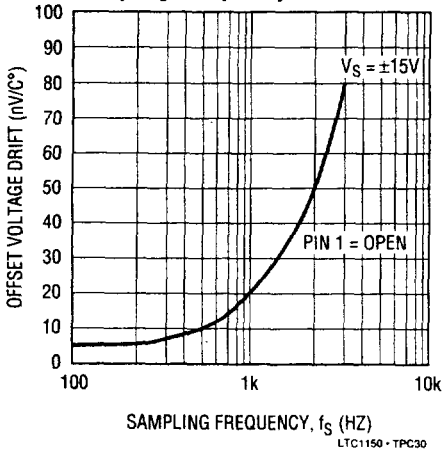

**PSRR vs Frequency**


POSITIVE SUPPLY, PIN 1 = OPEN
POSITIVE SUPPLY, PIN 1 = $V^-$
NEGATIVE SUPPLY, PIN 1 = OPEN
NEGATIVE SUPPLY, PIN 1 = $V^-$
PSRR (dB)
FREQUENCY (Hz)
LTC1150 • TPC29

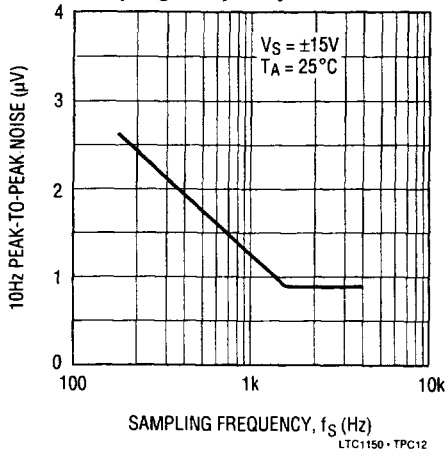
**Offset Voltage vs Sampling Frequency**



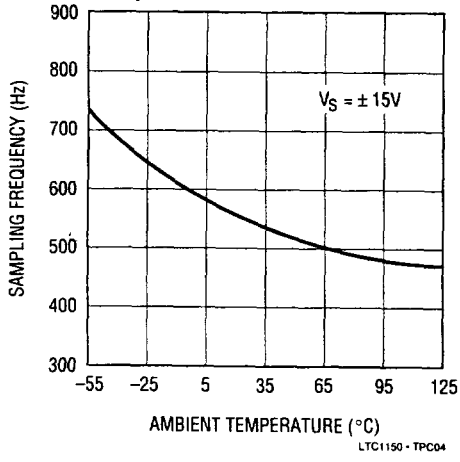

**Offset Voltage Drift vs Sampling Frequency**




**10Hz p-p Noise vs Sampling Frequency**

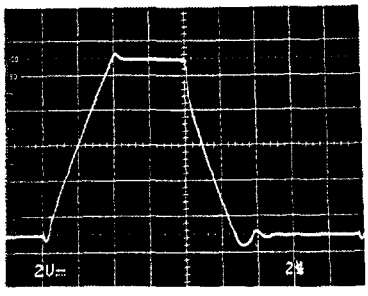



**Sampling Frequency vs Temperature**



# TYPICAL PERFORMANCE CHARACTERISTICS

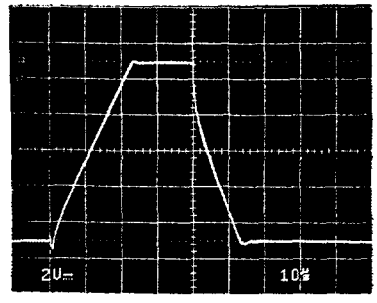
### Large Signal Transient Response




$V_S$ = ±15V, $A_V$ = 1, $C_L$ = 100pF, $R_L$ = 10kΩ

LTC1150 • TPC15

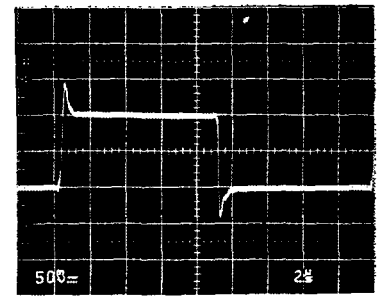
### Large Signal Transient Response, Pin 1 = $V^-$




$V_S$ = ±15V, $A_V$ = 1, $C_L$ = 100pF, PIN 1 = $V^-$

LTC1150 • TPC16

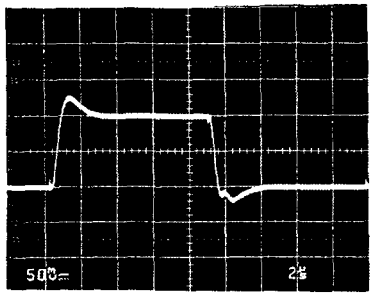
### Small Signal Transient Response




$V_S$ = ±15V, $A_V$ = 1, $C_L$ = 100pF, $R_L$ = 10kΩ

LTC1150 • TPC17

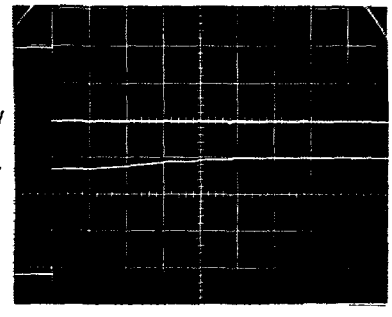
### Small Signal Transient Response, Pin 1 = $V^-$




$V_S$ = ±15V, $A_V$ = 1, $C_L$ = 100pF, $R_L$ = 10kΩ, PIN 1 = $V^-$

LTC1150 • TPC18

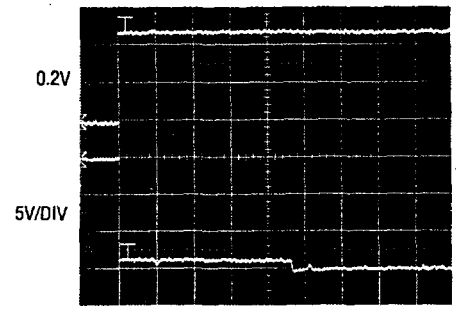
### Overload Recovery from Negative Saturation




$V_S$ = ±15V, $A_V$ = −100, 2ms/DIV

LTC1150 • TPC21

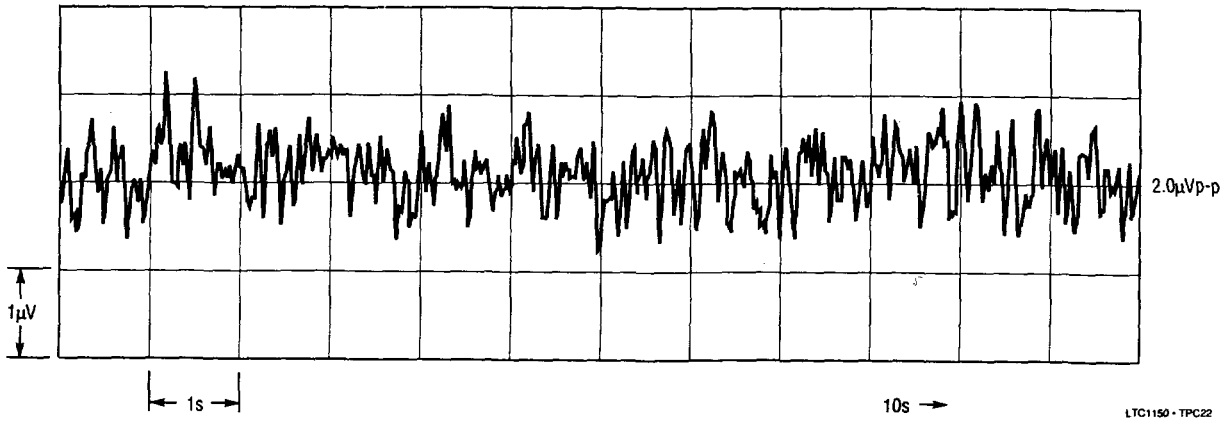
### Overload Recovery from Positive Saturation




$V_S$ = ±15V, $A_V$ = −100, 2ms/DIV

LTC1150 • TPC33

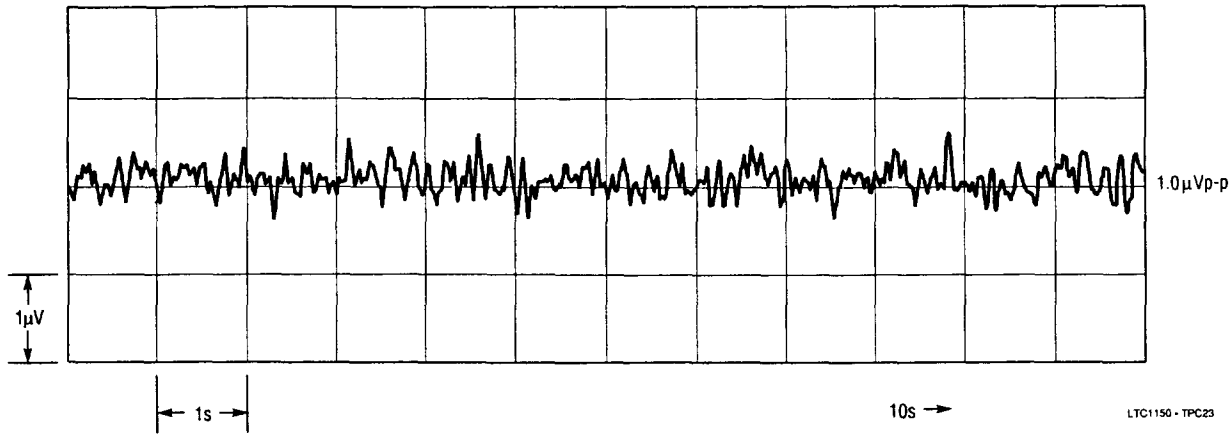
### 0.1Hz-10Hz Noise, V = ±15V, $T_A$ = 25°C, Internal Clock



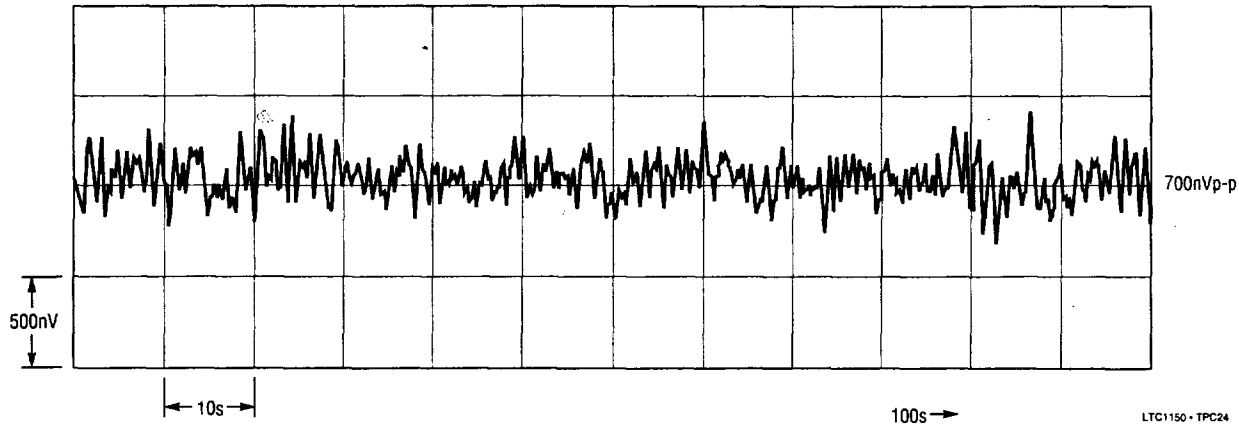

LTC1150 • TPC22

## TYPICAL PERFORMANCE CHARACTERISTICS

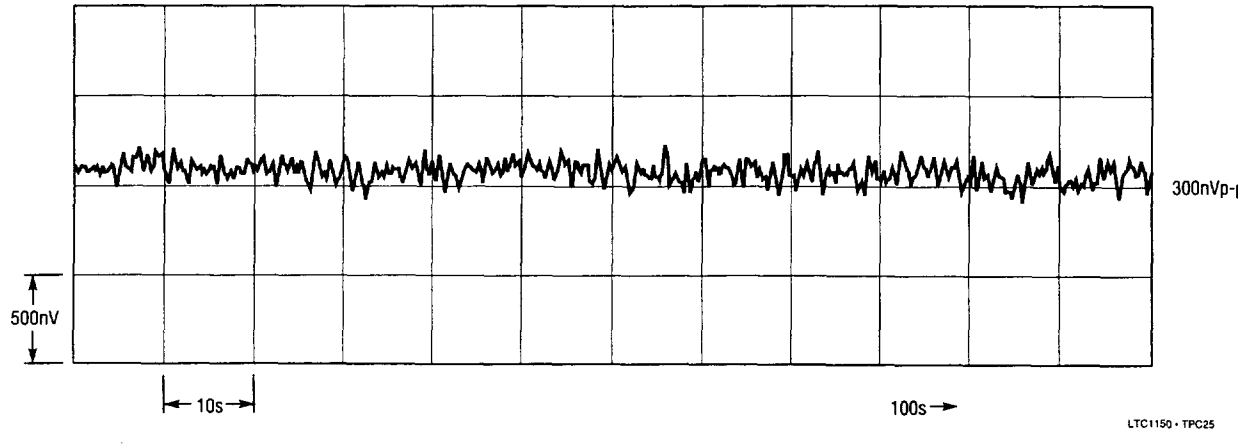
**0.1Hz-10Hz Noise, V = ±15V, $T_A$ = 25°C, $f_S$ = 1800Hz**




**0.1Hz-1Hz Noise, V = ±15V, $T_A$ = 25°C, Internal Clock**




**0.1Hz-1Hz Noise, V = ±15V, $T_A$ = 25°C, $f_S$ = 1800Hz**



## PIN DESCRIPTIONS

### 1) 8-Pin Packages

**Pin 1–** Supply Current Programming. The supply current can be programmed through pin 1. When pin 1 is left open or tied to $+V_S$, the supply current defaults to 800μA. Tying a resistor between pin 1 and pin 4, the negative supply pin, will reduce the supply current. The supply current, as a function of the resistor value, is shown in Typical Performance Characteristics.

**Pin 2 –** Inverting Input.

**Pin 3 –** Non-Inverting Input.

**Pin 4 –** Negative Supply.

**Pin 5 –** Optional External Clock Input. The LTC1150 has an internal oscillator to control the circuit operation of the amplifier if pin 5 is left open or biased at any DC voltage in the supply voltage range. When an external clock is desirable it can be applied to pin 5. The applied clock is AC-coupled to the internal circuitry to simplified interface requirements. The amplitude of clock input signal needs to be greater than 2V and the voltage level has to be within the supply voltage range. Duty cycle is not critical. The internal chopping frequency is the external clock frequency divided by four. When frequency of the external clock falls below 100Hz (internal chopping at 25Hz), the internal oscillator takes over and the circuit chops at 550Hz.

**Pin 6 –** Output.

**Pin 7 –** Positive Supply.

**Pin 8 –** Clock Output. The signal coming out of this pin is at the internal oscillator frequency of about 2.2kHz (four times the chopping frequency) and has voltage levels at $V_H = +V_S$ and $V_L = V_S - 4.6V$. If the circuit is driven by an external clock, pin 8 is pulled up to $+V_S$.

## APPLICATIONS INFORMATION

### ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

#### Picoamperes

In order to realize the picoampere level of accuracy of the LTC1150, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary – particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations the guard ring should be tied to ground; in non-inverting connections to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

#### Microvolts

Thermocouple effects must be considered if the LTC1150's ultra low drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect if a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C — four times the maximum drift specification of the LTC1150. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C — 700 times the maximum drift specification of the LTC1150.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and

## APPLICATIONS INFORMATION

component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

Figure 1 is an example of the introduction of an unnecessary resistor to promote differential thermal balance. Maintaining compensating junctions in close physical proximity will keep them at the same temperature and reduce thermal EMF errors.

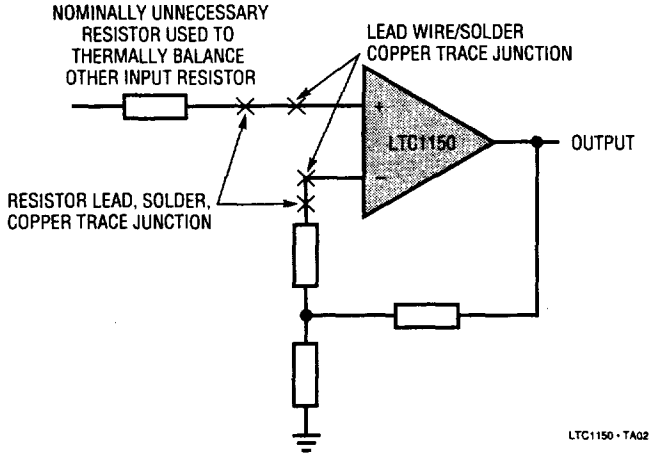

NOMINALLY UNNECESSARY RESISTOR USED TO THERMALLY BALANCE OTHER INPUT RESISTOR
LEAD WIRE/SOLDER COPPER TRACE JUNCTION
LTC1150
OUTPUT
RESISTOR LEAD, SOLDER, COPPER TRACE JUNCTION
LTC1150 • TA02

**Figure 1. Extra Resistors Cancel Thermal EMF**

When connectors, switches, relays and/or sockets are necessary they should be selected for low thermal EMF activity. The same techniques of thermally-balancing and coupling the matching junctions are effective in reducing the thermal EMF errors of these components.

Resistors are another source of thermal EMF errors. Table 1 shows the thermal EMF generated for different resistors. The temperature gradient across the resistor is important, not the ambient temperature. There are two junctions formed at each end of the resistor and if these junctions are at the same temperature, their thermal EMFs will cancel each other. The thermal EMF numbers are approximate and vary with resistor value. High values give higher thermal EMF.

**Table 1. Resistor Thermal EMF**

| Resistor Type | Thermal EMF/°C Gradient |
|---|---|
| Tin Oxide | ~mV/°C |
| Carbon Composition | ~450μV/°C |
| Metal Film | ~20μV/°C |
| Wire Wound | |
| Evenohm | ~2μV/°C |
| Manganin | ~2μV/°C |

### PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1150's offset nulling loop and cannot be cancelled. Metal can H packages exhibit the worst warm-up drift. The input offset voltage specification of the LTC1150 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

### ALIASING

Like all sampled data systems, the LTC1150 exhibits aliasing behavior at input frequencies near the sampling frequency. The LTC1150 includes a high-frequency correction loop which minimizes this effect; as a result, aliasing is not a problem for most applications.

For a complete discussion of the correction circuitry and aliasing behavior, please refer to the LTC1051/53 data sheet.

### SYNCHRONIZATION OF MULTIPLE LTC1150's

When synchronization of several LTC1150's is required, one of the LTC1150's can be used to provide the "master" clock to control over 100 "slave" LTC1150's. The master clock, coming from pin 8 of the master LTC1150, can directly drive pin 5 of the slaves. Note that pin 8 of the slave LTC1150's will be pulled up to $+V_S$.

If all the LTC1150's are to be synchronized with an external clock, then the external clock should drive pin 5 of all the LTC1150's.

## APPLICATIONS INFORMATION

### LEVEL SHIFTING THE CLOCK

Level shifting is needed if the clock output of the LTC1150 in ±15V operation must interface to regular +5V logic circuits. Figures 2 and 3 show some typical level shifting circuits.

When operated from a single +5V or ±5V supplies, the LTC1150 clock output at pin 8 can interface to TTL or CMOS inputs directly.

### LOW SUPPLY OPERATION

The minimum supply for proper operation of the LTC1150 is typically below 4.0V (±2.0V). In single supply applications, PSRR is guaranteed down to 4.7V (±2.35V) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

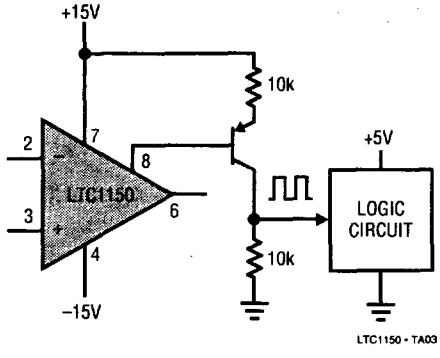



Figure 2. Output Level Shift (Option 1)

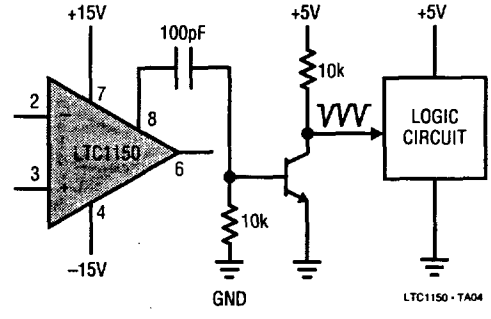
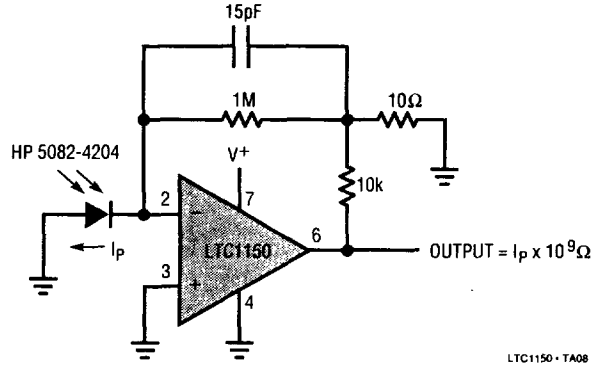


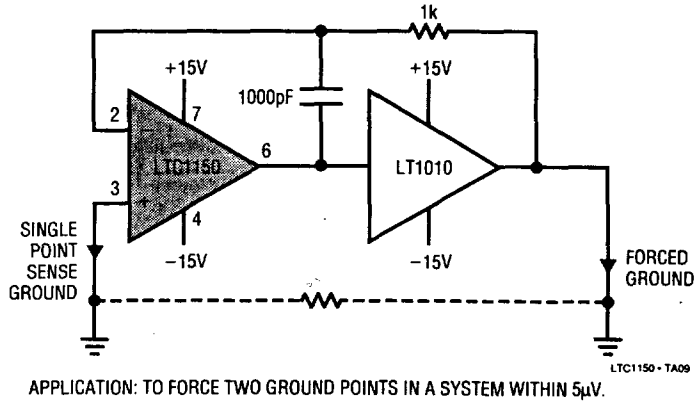

Figure 3. Output Level Shift (Option 2)

## TYPICAL APPLICATIONS

**Low Level Photodetectector**



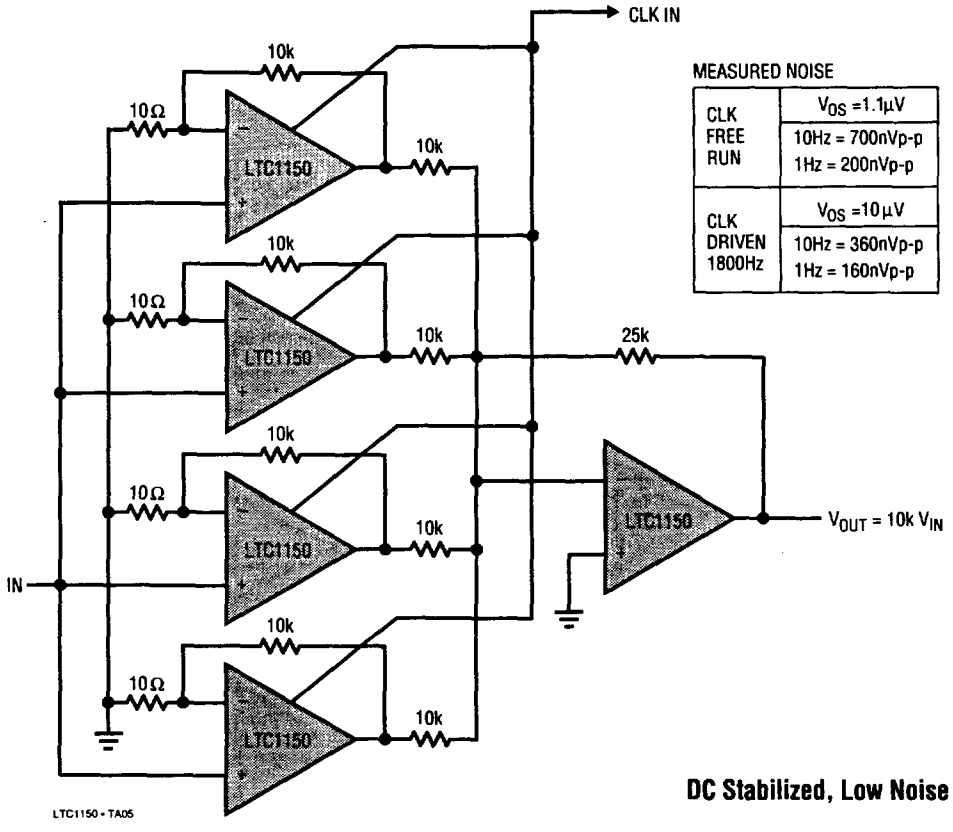

**Ground Force Reference**




APPLICATION: TO FORCE TWO GROUND POINTS IN A SYSTEM WITHIN 5μV.

# TYPICAL APPLICATIONS

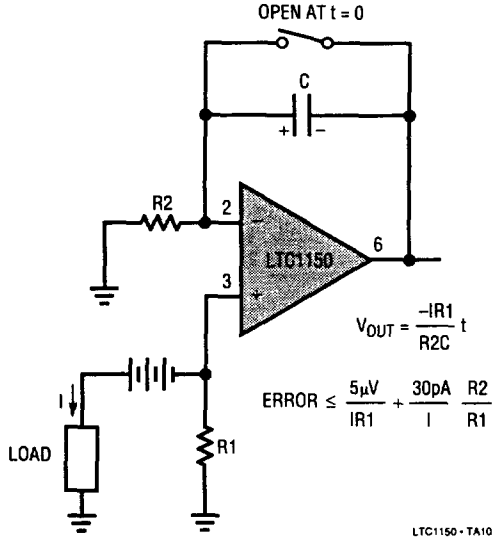
### Paralleling to Improve Noise




MEASURED NOISE

| | |
|---|---|
| CLK FREE RUN | $V_{OS}$ =1.1μV |
| | 10Hz = 700nVp-p |
| | 1Hz = 200nVp-p |
| CLK DRIVEN 1800Hz | $V_{OS}$ =10μV |
| | 10Hz = 360nVp-p |
| | 1Hz = 160nVp-p |

### Battery Discharge Monitor




### DC Stabilized, Low Noise Amplifier